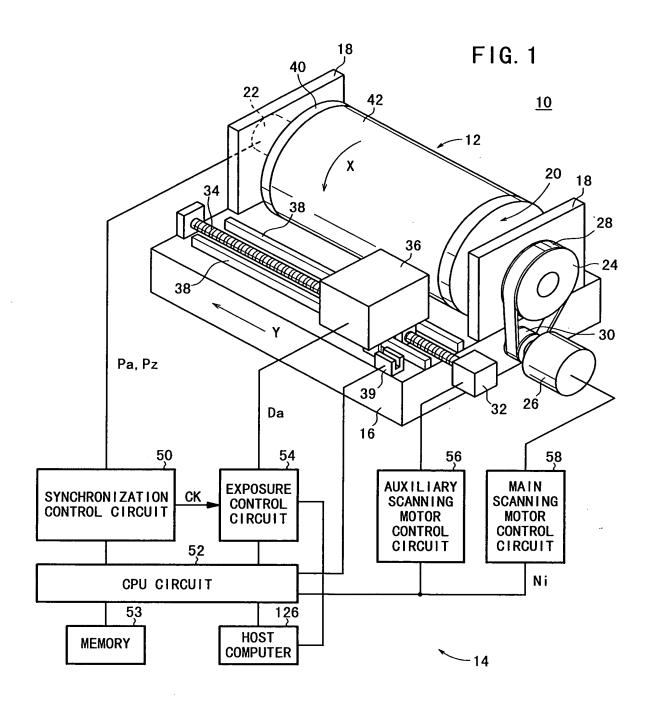


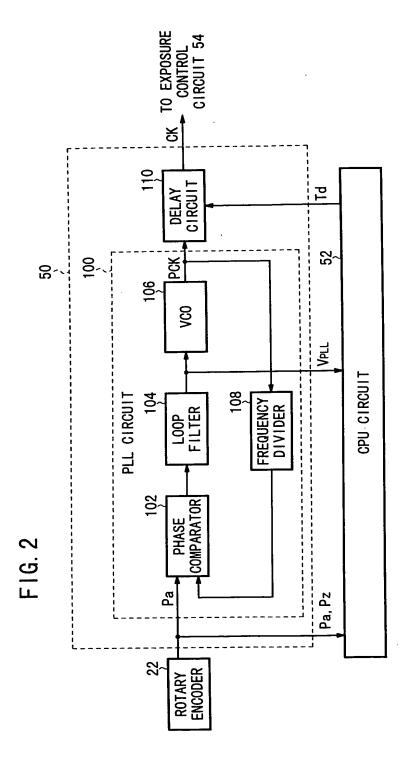
Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002

Darryl Mexic 1 of 22

202-293-7060

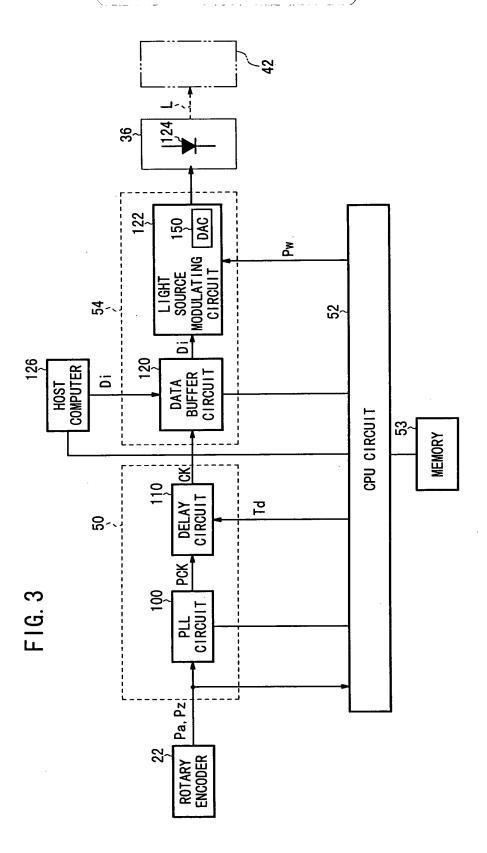


Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 2 of 22





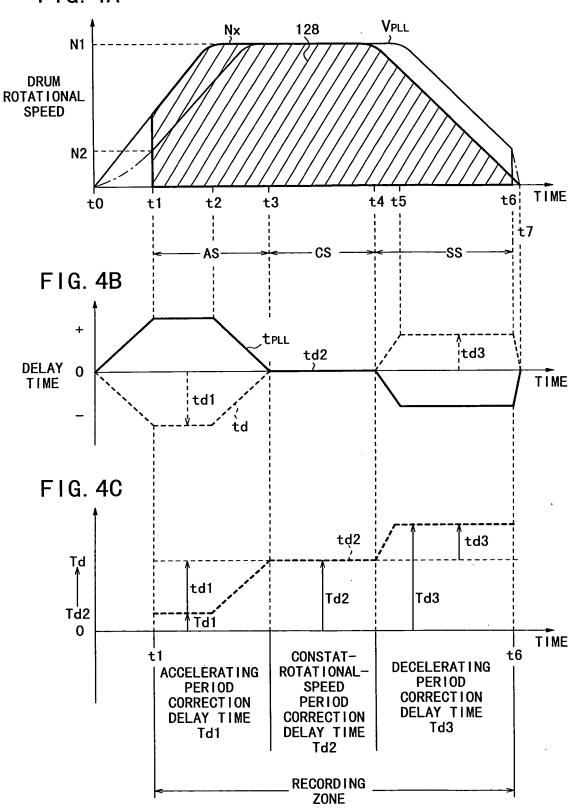
Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 3 of 22



Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060

4 of 22







U6/364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2000 CQ67364 Filed: January 16, 2002

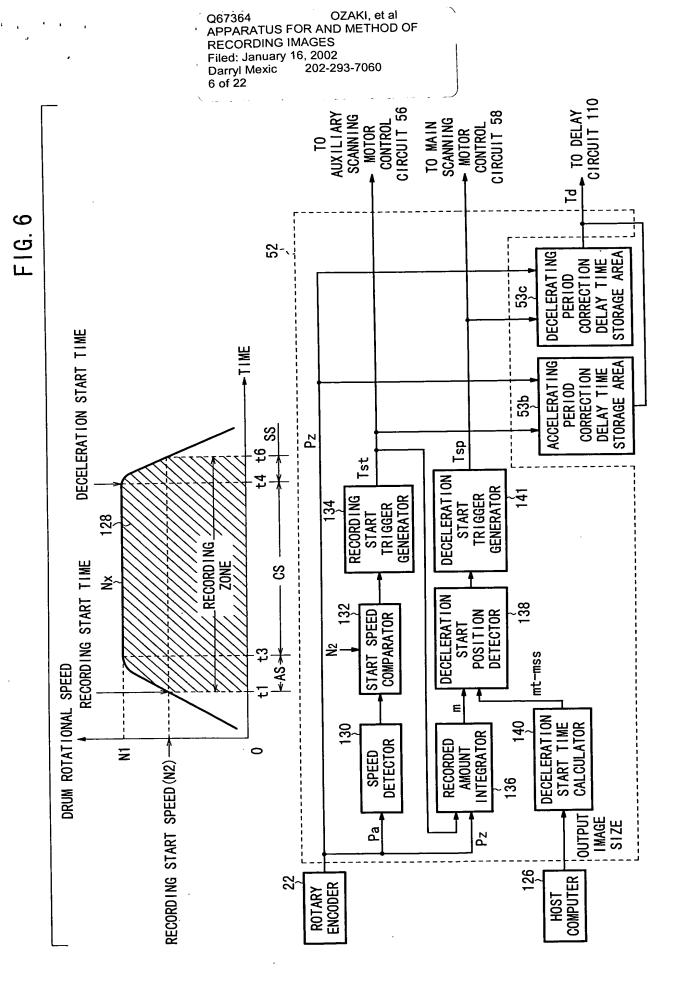
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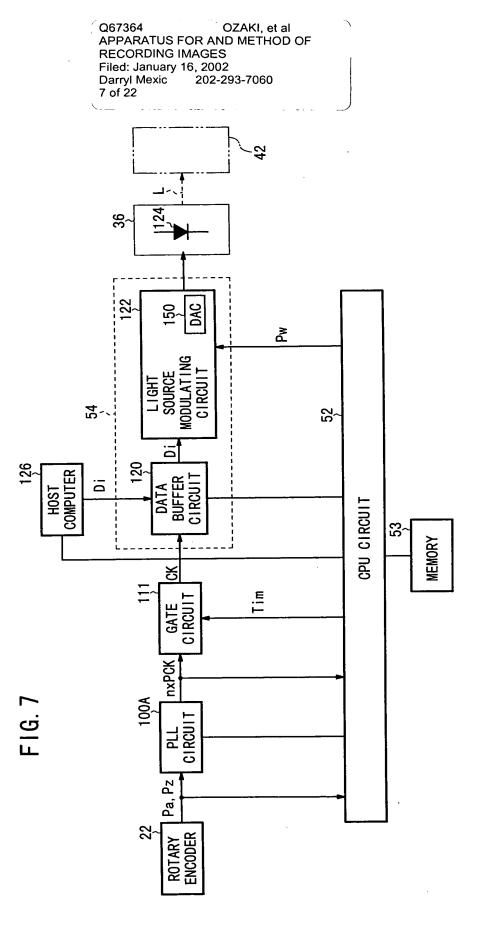
Darryl Mexic 5 of 22

FIG. 5

53

			53	
ST	ORAGE AREA	ADDRESS	DATA	
53a	BASIC DELAY TIME DATA td	ADa I ADb	td1 td2 1 td3	
53b	ACCELERATING PERIOD CORRECTION DELAY TIME	ADc ADd	Td1 Td2	
53c	DECELERATING PERIOD CORRECTION DELAY TIME	ADe ADf	Td2 Td3	
53d	ACCELERATING PERIOD LASER OUTPUT	ADg ADh	Pwa I Pwc	
53e	DECELERATING PERIOD LASER OUTPUT	ADi I ADj	Pwc 	





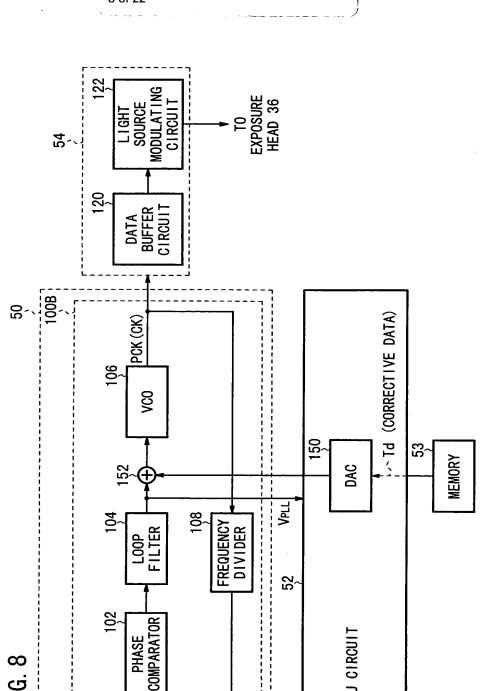
Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 8 of 22

PHASE

22

ROTARY ENCODER

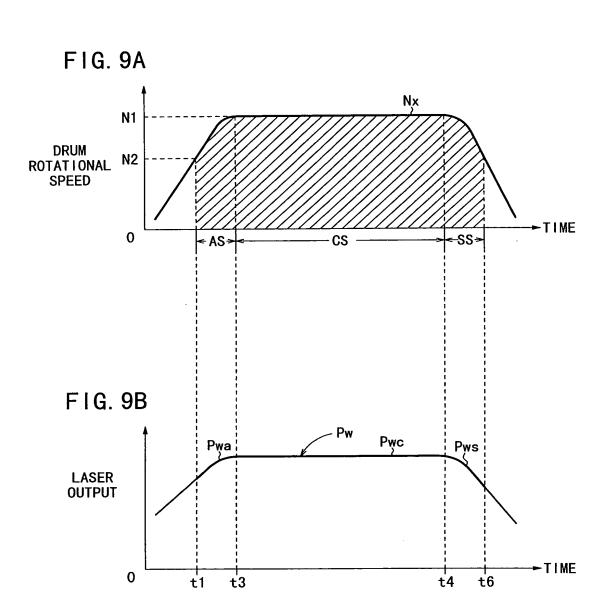
F1G. 8

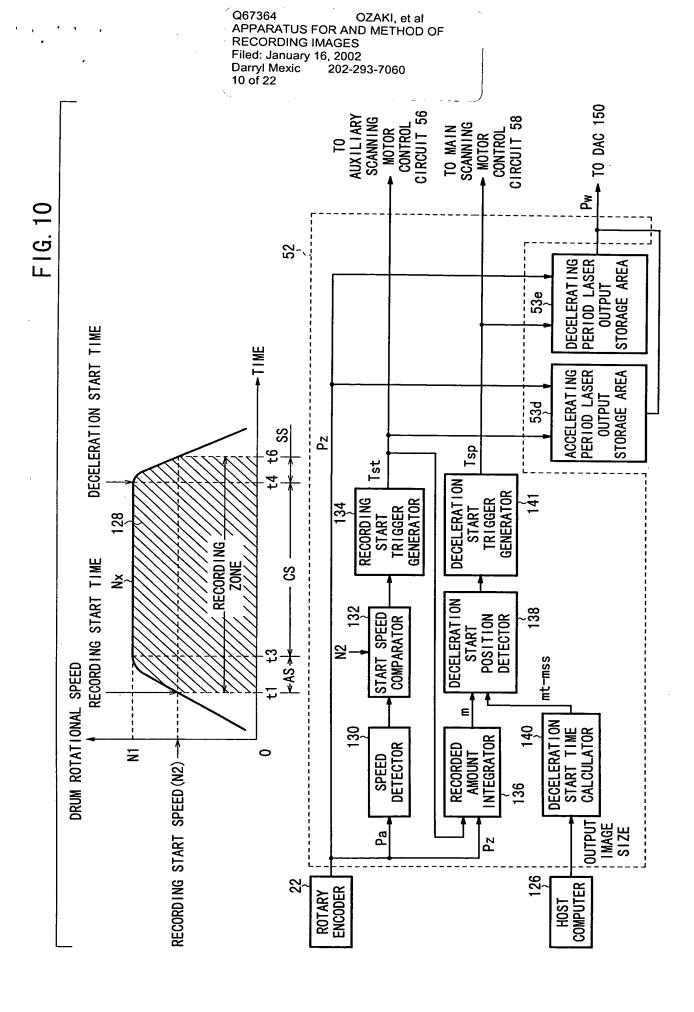


CPU CIRCUIT

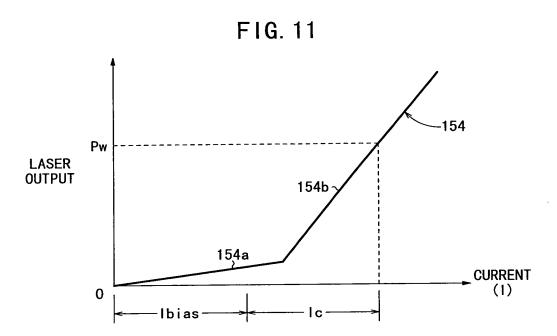
Pa, Pz

Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 9 of 22



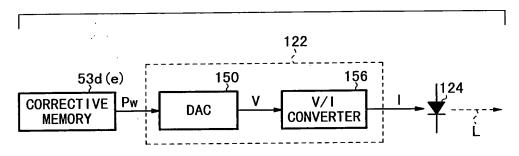


Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 11 of 22

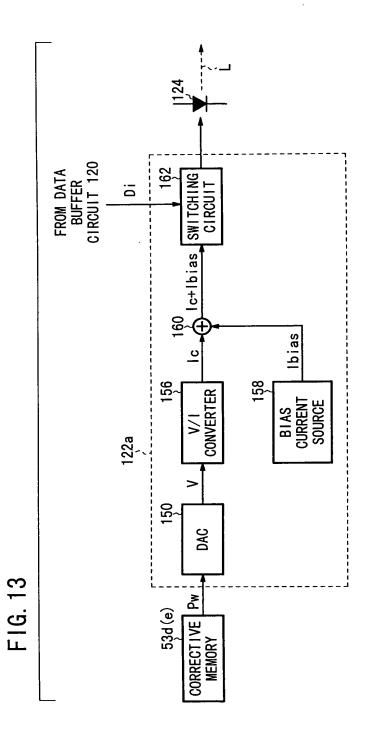


Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 12 of 22

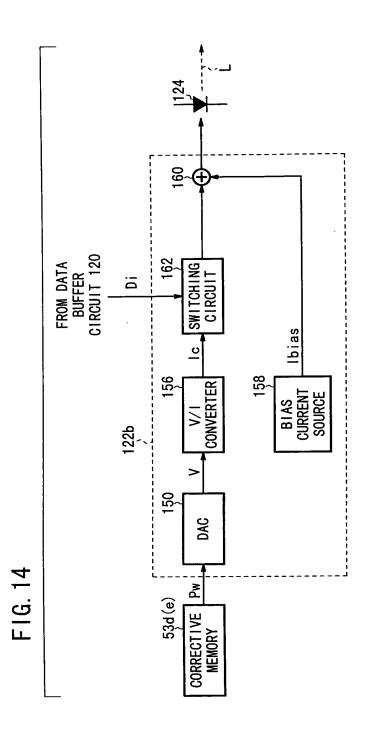
FIG. 12



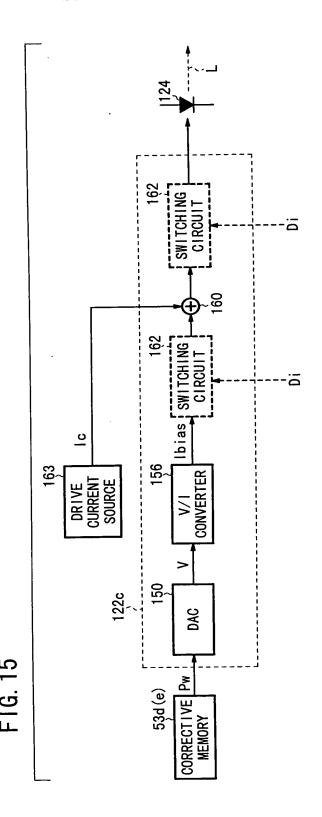
Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 13 of 22



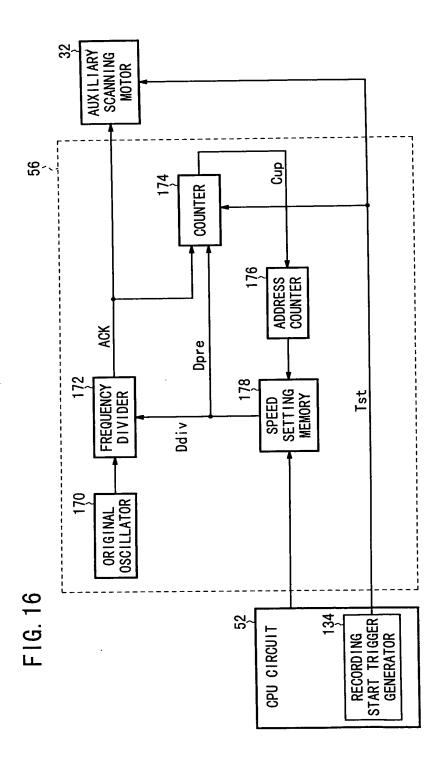
Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 14 of 22



Q67364 OZAKI, et all PPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 15 of 22



Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 16 of 22

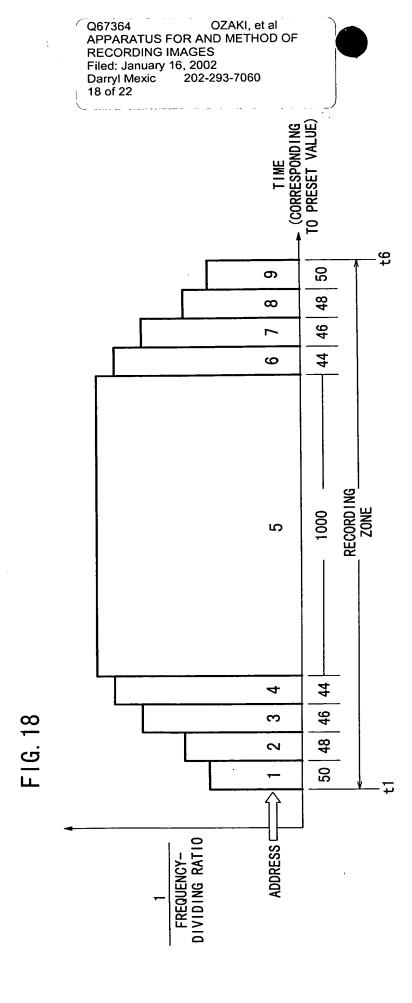


Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 17 of 22

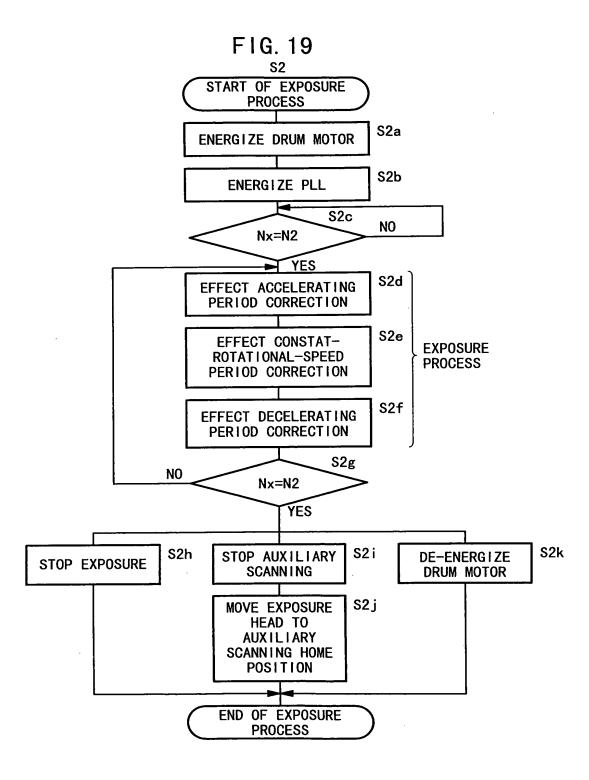
FIG. 17

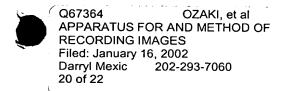
178

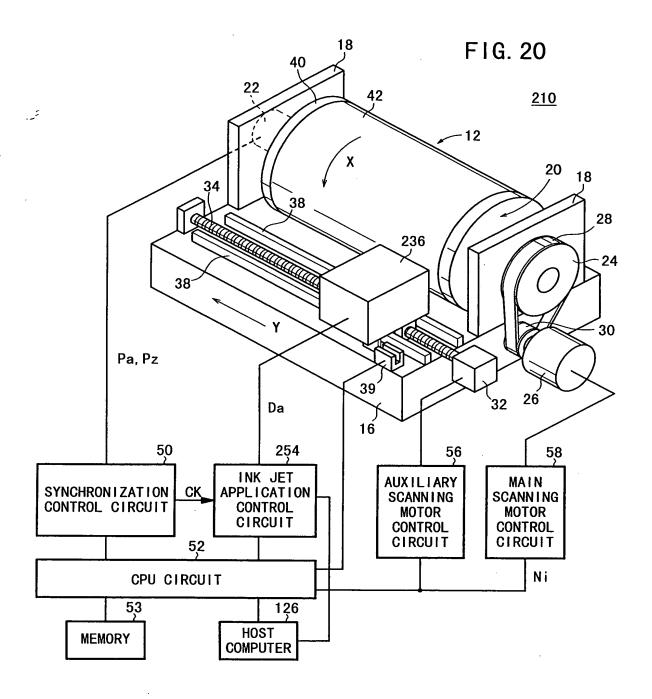
ADDRESS	FREQUENCY- DIVIDING RATIO (Ddiv)	PRESET VALUE (Dpre)	APPARATUS OPERATING STATUS
1	100	50	ACCELERATION STARTED
2	95	48	IN ACCELERATION
3	90	46	DITTO
4	85	44	DITTO
5	80	1000	AT CONSTANT SPEED
6	85	44	DECELERATION STARTED
7	90	46	IN DECELERATION
8	95	48	DITTO
9	100	50	DECELERATION ENDED



Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060 19 of 22









Q67364 OZAKI, et al APPARATUS FOR AND METHOD OF RECORDING IMAGES Filed: January 16, 2002 Darryl Mexic 202-293-7060

21 of 22

FIG. 21 PRIOR ART

